REMARKS

Claims 37-40, 42, 43 and 53-63 were pending in the application. By this paper, Applicant has amended Claims 37-40, 42, 43 and 53-63 and added new Claims 64-83. Accordingly, Claims 37-40, 42, 43 and 53-83 are presented herein for examination.

Rejections under §112, Second Paragraph

In response to the Examiner Section 112, second paragraph rejections of Claims 37-40, 42-43, 53-58, 60-61 and 63 (see Pars. 3-19 of the Office Action), Applicant has herein amended each of the foregoing claims to overcome the Examiner's rejections. Applicant respectfully requests that all such rejections now be withdrawn.

Rejections Under 35 U.S.C. §103

Claims 39 and 40 - Claims 39 and 40 were rejected by the Examiner under Section 103 over Lee in view of Wirthlin (see par. 21 of the Office Action). By this paper, Applicant has amended Claims 39 and 40 to include limitations relating to the user-customized processor core configuration being rendered in a hardware description language model. Support for this amendment is found at, *inter alia*, pages 13-15 of the specification as filed generally (discussing Fig. 4), and U.S. Patent 6,862,563, which was incorporated by reference into the instant application in its entirety.

Applicant respectfully submits that not only does Wirthlin *not* teach or suggest use of a hardware description language (HDL) representation of the processor core that integrates the instruction set and extension instruction, it also *teaches away* from such integration (and use of an HDL model). Specifically, page 23, Section 1 ("Introduction"), Col. 2 of Wirthlin states:

> "*...most reconfigurable systems are programmed using conventional hardware development techniques such as schematic capture or hardware description languages.[2] As the number of FPGAs in reconfigurable systems increases, the task of developing custom circuits for each FPGA in the system becomes enormous.*" {emphasis added}

As evidenced in the foregoing cite and the balance of Wirthlin, the processor of Wirthlin is implemented using a plurality of reconfigurable logic FPGAs. Wirthlin states in the above citation that as the number of these FPGAs in a given system increases, the ability to use conventional approaches such as schematic capture or hardware description languages (HDL) becomes unwieldy. Hence, Wirthlin purposely avoids using such conventional approaches, including HDL, since they require an innate knowledge by the user/designer (see, e.g., page 26, Section 3.1.3, Col. 1, first par. of Wirthlin, wherein the desire to create "re-usable" processors to avoid the creation of "custom processors" is described).

Accordingly, the generation of a customized HDL model as in Applicant's claimed invention runs completely counter to Wirthlin's intentions and teachings.

This fact is further borne out by Wirthlin's teachings on page 27, Section 3.4, Col. 2 (second full paragraph), wherein it is stated that:

> "*Custom instructions are developed as separate modules using conventional schematic entry or synthesis methods.*" {emphasis added}

See also page 25, Section 3.1.2., Col. 2 of Wirthlin, discussing how most of the FPGA resources are available for custom instruction specification after the nP core design has been determined ("minimized"). Hence, Wirthlin teaches an approach where a static and non-custom core is specified using FPGA assets, and then a "custom instruction set" is specified afterward and separately using the remainder of the FPGA assets. This is in stark contrast to Applicant's claimed invention, wherein the recited extension instruction is integrated into a common hardware description language (HDL) model of the processor. **Applicant's inventions of Claims 39 and 40 comprise the quintessence of a "customized processor", precisely what Wirthlin teaches away from and seeks to avoid.**

Hence, Wirthlin cannot as a matter of law be combined with the other references cited by the Examiner to render the invention of Claims 39 or 40 obvious, since Wirthlin explicitly teaches away from such combination.

Claims 37-40 and 62-63 - By this paper, independent Claims 37-40 and 62-63 have been amended to include limitations relating to the recited processor core being user-customized (customizable). As noted above, Wirthlin (used as the basis for the Examiner's rejections of Claims 37-40) explicitly teaches away from a user-customized core; see page 26, first par. of Col. 1 wherein it is stated:

> "*Hardware processors for a class of applications can be reused so users do **not** have to create **a custom processor** for each application.*"

As previously discussed, this is the antithesis of Applicant's claimed inventions, which necessarily require user input regarding customization of the processor (core).

Regarding Claims 62 and 63, Applicant notes that a user-customized processor/core is now recited. Neither Lee nor Wirthlin in any way teach or suggest a processor or core, and in fact Wirthlin teaches away from such functionality as discussed herein, *supra.*

Regarding Lee, what the Examiner relies upon as being "user-configurable" are the instructions, and not the core configuration itself; see page 17, par. 35, lines 16-19 ("Finally,...") of the Office Action. Lee in no way teaches or suggests that the processor or core itself is user-configurable at the time of design.

Hence, neither Wirthlin nor Lee as a matter of law can be combined with the other references cited by the Examiner to render the invention of Claims 37-40 and 59-63 obvious, since Wirthlin explicitly teaches away from such combination, and Lee makes no teaching or suggestion of user-configurability of the core design.

Claim 59 – By this paper, Claim 59 has been amended to include limitations relating to the recited processor (core) having a configuration determined at least in part by said user-customization and user-extension at the time of its design. As discussed herein *supra*, none of the cited art (including Lee) teaches or suggests such functionality. Lee teaches or suggests nothing regarding user-customization or extension at time of design, nor does Heuring. Hence, these references cannot be combined to render Applicant's claimed invention obvious.

Claims 60 and 61 – By this paper, Claims 60 and 61 have been amended to include limitations relating to the recited processor being generated from a hardware description language model. As discussed herein *supra*, none of the cited art (including Lee) teaches or suggests such functionality. Lee teaches or suggests nothing regarding use of a description language model to generate its processor, nor does Heuring. Hence, these references cannot be combined to render Applicant's claimed inventions obvious.

New Claims

By this paper, Applicant has added new independent Claims 64-67, as well as 68, 72, 76, and 80.

New Claims 64-67 correspond generally to existing Claims 37-40 respectively, and include limitations relating to the recited processor core being user-customized at time of its design. None of the cited art teaches or suggest such functionality in combination with the other limitations of these claims.

New Claims 68, 72, 76, and 80 also correspond generally to existing Claims 37-40 respectively, and include limitations relating to the user-configuration process, as set forth on pages 13-15 generally (discussing Fig. 4), and U.S. Patent 6,862,563, which was incorporated by reference into the instant application in its entirety. Applicant submits that none of the cited art proffered by the Examiner (including Lee and Wirthlin) teach or suggest the aforementioned limitations, let alone all limitations claimed in Claims 68, 72, 76, and 80.

Accordingly, Applicant submits that Claims 68, 72, 76, and 80 define patentable subject matter and are in condition for allowance.

Other Remarks

Applicant hereby specifically reserves the right to prosecute claims of different or broader scope, including those cancelled without prejudice herein, in a continuation or divisional application, as well as its rights of appeal.

Applicant notes that any cancellations or additions made herein are made solely for the purposes of more clearly and particularly describing and claiming the invention, and not for purposes of overcoming art or for reasons relating to patentability unless otherwise stated. The Examiner should infer no (i) adoption of a position with respect to patentability, (ii) change in the Applicant's position with respect to any claim or subject matter of the invention, or (iii) acquiescence in any way to any position taken by the Examiner, based on such cancellations or additions.

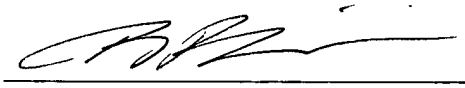
Furthermore, any remarks made with respect to a particular claim or claims shall be solely limited to only such claim or claims.

If the Examiner has any questions or comments which may be resolved over the telephone, he is requested to call the undersigned at (858) 675-1670.

Respectfully submitted,

GAZDZINSKI & ASSOCIATES

Dated: March 28, 2005

By: 

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